WHAT IS CLAIMED IS:

1. A method of forming semiconductor transistors, comprising:

forming a gate electrode over but insulated from a semiconductor body region;

forming off-set spacers along side-walls of the gate electrode; and

after forming said off-set spacers, forming a source region and a drain region in the body region so that the extent of an overlap between the gate electrode and each of the source and drain regions is dependent on a thickness of the off-set spacers.

2. The method of claim 1 wherein said gate electrode forming act includes forming a gate electrode for each of first and second transistors, and said off-set spacers forming act includes forming off-set spacers along side-walls of the gate electrodes of the first and second transistors, said source and drain regions forming act further comprising:

performing a DDD implant to form DDD source and DDD drain regions for the first transistor.

3. The method of claim 2 further comprising:

after said DDD implant, forming main spacers adjacent the off-set spacers of the first and second transistors or of the second transistor only;

after forming said main spacers, performing a LDD implant to form LDD source and LDD drain regions for the second transistor; and

after forming the main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and DDD source regions and each of the LDD drain and LDD source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

4. The method of claim 3 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions is inversely dependent on a thickness of the off-set spacers,

the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacer only, and

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers.

5. The method of claim 2 further comprising:

performing a LDD implant to form LDD source and LDD drain regions for the second transistor;

after both said DDD and LDD implants, forming main spacers adjacent the off-set spacers of the first and second transistors; and

after forming said main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and DDD source regions and each of the LDD drain and LDD source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

6. The method of claim 5 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions, and the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers, and

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers.

7. The method of claim 5 wherein N^- type impurities is used in each of the DDD and LDD implants, and N^+ type impurities is used in the S/D implant.

8. The method of claim 5 wherein P^- type impurities is used in each of the DDD and LDD implants, and P^+ type impurities is used in the S/D implant.

9. The method of claim 1 wherein said gate electrode forming act includes forming a gate electrode for each of first and second transistors, and said off-set

spacers forming act includes forming off-set spacers along side-walls of the gate electrodes of the first and second transistors, said source and drain regions forming act further comprising:

performing a LDD implant to from LDD source and LDD drain regions for the second transistor.

10. The method of claim 9 further comprising:

prior to forming the off-set spacers, performing a DDD implant to from DDD source and DDD drain regions in the body region for the first gate electrode;

after said LDD implant, forming main spacers adjacent the off-set spacers of the first and second transistors or of the first transistor only; and

after forming the main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and source regions and the LDD drain and source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

11. The method of claim 10 wherein,

the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacer only, and

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers.

12. The method of claim 1 wherein the off-set spacers are from oxide or oxynitride.

13. The method of claim 1 wherein,

said off-set spacers forming act further comprises forming a layer of insulating material over the gate electrode including the side-walls of the gate electrode, and over exposed areas of the body region; and

said source and drain regions forming act further comprises implanting impurities through the insulating layer to form said source and drain regions.

14. The method of claim 1 wherein the off-set spacers forming act further comprises:

forming a first layer of insulating material over the gate electrode and the body region;

forming a second layer of insulating material different from the first layer of insulating material over the first layer of insulating material; and

etching at least one of the first and second layers of insulating material to form the off-set spacers along the side-walls of the gate electrode.

15. The method of claim 14 wherein the first layer of insulating material is oxide and the second layer of insulating material is nitride, the etching act further comprising:

etching both first and second layers of insulating material so that only oxide-nitride off-set spacers remain along the side-walls of the gate electrode.

16. The method of claim 14 wherein the first layer of insulating material is oxide and the second layer of insulating material is nitride, the etching act further comprising:

etching only the nitride layer so that oxide-nitride off-set spacers are formed along the side-walls of the gate electrode while only the nitride is removed from all other areas.

17. The method of claim 16 further comprising:

after said nitride layer etching act, implanting impurities through the oxide layer to form said source and drain regions.

18. The method of claim 1 wherein thicker off-set spacers result in smaller overlap between the gate electrode and each of the source and drain regions.

19. A method of forming a non-volatile memory cell, comprising:

forming a first polysilicon layer over but insulated from a semiconductor body region;

forming a second polysilicon layer over but insulated from the first polysilicon layer;

forming an off-set spacer along at least one side-wall of the first and second polysilicon layers; and

after forming said off-set spacer, forming at least one of source and drain regions in the body region so that the extent of an overlap between the first polysilicon layer and said one of source and drain regions is dependent on a thickness of the off-set spacer.

20. The method of claim 19 wherein the first and second polysilicon layers form a polysilion stack, off-set spacers being formed along side-walls of the polysilicon stack, and source and drain regions being formed after forming the off-set spacers so that the extent of an overlap between the polysilicon stack and each of the source and drain regions is inversely dependent on a thickness of the off-set spacers.

21. The method of claim 19 where the non-volatile memory cell is a split gate cell.

22. The method of claim 19 wherein the first and second polysilicon layers form a polysilion stack, the off-set spacers being formed along side-walls of the polysilicon stack, the act of forming at least one of source and drain regions further comprising:

performing a DDD implant to form a DDD source region.

23. The method of claim 22 further comprising:

performing a source/drain (S/D) implant to form a drain region and to form a highly doped region within the DDD source region, the highly doped region being of the same conductivity type as and having a doping concentration greater than the DDD source region, wherein the extent of an overlap between the stack of first and second polysilicon layers and each of the DDD source region, the highly doped region within the DDD source region, and the drain region is inversely dependent on a thickness of the off-set spacers.

24. The method of claim 19 further comprising:

prior to forming the off-set spacer, performing a DDD implant to form a DDD source region.

25. The method of claim 24 wherein the first and second polysilicon layers form a polysilion stack,

the off-set spacer forming act further comprising forming off-set spacers along side-walls of the stack of first and second polysilicon layers, and

the forming at least one of source and drain regions further comprises performing a source/drain (S/D) implant to form a drain region and to form a highly doped region within the DDD source region, the highly doped region being of the same conductivity type as and having a doping concentration greater than the DDD source region, wherein the extent of an overlap between the stack of first and second polysilicon layers and each of the drain region and the highly doped region within the DDD source region is inversely dependent a thickness of the off-set spacers, and a distance between an outer edge of the DDD source region and the highly doped region within the DDD source region is directly dependent on the thickness of the off-set spacers.

26. The method of claim 25 wherein N^- type impurities is used in the DDD implant, and N^+ type impurities is used in the S/D implant.

27. The method of claim 25 wherein P^- type impurities is used in the DDD implant, and P^+ type impurities is used in the S/D implant.

28. The method of claim 19 wherein the off-set spacer is from oxide or oxynitride.

29. The method of claim 19 wherein the first and second polysilicon layers form a polysilion stack,

said off-set spacer forming act further comprising forming a layer of insulating material over the polysilicon stack including the side-walls of the polysilicon stack, and over the body region, and

said at least one source and drain regions forming act further comprising implanting impurities through the insulating layer to form said source and drain regions.

30. The method of claim 19 wherein the first and second polysilicon layers form a polysilion stack, the off-set spacer forming act further comprising:

forming a first layer of insulating material over the polysilicon stack and exposed areas of the body region;

forming a second layer of insulating material different from the first layer of insulating material over the first layer of insulating material; and

etching at least the second layer of insulating material to form off-set spacers along the side-walls of the polysilicon stack.

31. The method of claim 30 wherein the first layer of insulating material is oxide and the second layer of insulating material is nitride, the etching act further comprising:

etching first and second layers of insulating material so that only oxide-nitride off-set spacers remain along the side-walls of the polysilicon stack.

32. The method of claim 30 wherein the first layer of insulating material is oxide and the second layer of insulating material is nitride, the etching act further comprising:

etching only the nitride layer so that oxide-nitride off-set spacers are formed along the side-walls of the polysilicon stack while the nitride is removed from all other areas.

33. The method of claim 32 further comprising:

after said nitride layer etching act, implanting impurities through the oxide layer to form said at least one of source and drain regions.

34. The method of claim 19 wherein a thicker off-set spacer results in a smaller overlap between the first polysilicon layer and said at least one of source and drain regions.

35. A method of forming a non-volatile memory cell and transistors, comprising:

forming a first polysilicon layer over but insulated from a semiconductor body region, and a second polysilicon layer over but insulated from the first polysilicon layer, the first and second polysilicon layers forming a polysilicon stack of the memory cell;

forming a gate electrode for each of first and second transistors over but insulated from a semiconductor region;

forming off-set spacers along side-walls of the polysilicon stack and the gate electrode of the first and second transistors; and

after forming said off-set spacers, forming source and drain regions for each of the memory cell and the first and second transistors so that the extent of an overlap between the polysilicon stack and the cell source and drain regions and the extent of an overlap between each of the gate electrodes of the first and second transistors and their corresponding source and drain regions are dependent on a thickness of the off-set spacers.

36. The method of claim 35 wherein said source and drain forming act further comprises:

performing a source/drain (S/D) implant to simultaneously form the source and drain regions of each of the memory cell and the first and second transistors.

37. The method of claim 35 wherein the gate electrodes of the first and second transistors are formed simultaneously with the second polysilicon layer.

38. The method of claim 35 further comprising:

performing a DDD implant to form DDD source and DDD drain regions for the first transistor; and

performing a LDD implant to form LDD source and LDD drain regions for the second transistor.

39. The method of claim 38 wherein said LDD implant is performed after said DDD implant, the method further comprising:

after said DDD implant but before said LDD implant, forming main spacers adjacent the off-set spacers of at least the first transistor.

40. The method of claim 39 further comprising:

after said LDD implant, performing a source/drain (S/D) implant to form at least one of:

(a) cell source and cell drain regions, and

(b) highly doped regions within all the DDD and LDD regions,

wherein the highly doped regions within all the DDD and LDD regions are of the same conductivity type as and have a doping concentration greater than the DDD and LDD regions.

41. The method of claim 40 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions is inversely dependent on a thickness of the off-set spacers,

the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacers only,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers, and

the extent of an overlap between the polysilicon stack and the cell source and drain regions is inversely dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacers only.

42. The method of claim 40 further comprising:

forming a cell DDD source region during said DDD implant so that said S/D implant forms a highly doped region within the cell DDD source region.

43. The method of claim 38 further comprising:

after both said DDD implant and said LDD implant, forming main spacers adjacent the off-set spacers of at least the first and second transistors.

44. The method of claim 43 further comprising:

after said main spacers forming act, performing a source/drain (S/D) implant to form at least one of:

(a) cell source and cell drain regions, and

(b) highly doped regions within all the DDD and LDD regions.

wherein the highly doped regions within all the DDD and LDD regions are of the same conductivity type as and have a doping concentration greater than the DDD and LDD regions.

45. The method of claim 44 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions, and the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers,

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers,

and the extent of an overlap between the polysilicon stack and the cell source and drain regions is inversely dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacers only.

46. The method of claim 44 further comprising:

forming a cell DDD source region during said DDD implant so that said S/D implant forms a highly doped region within the cell DDD source region.

47. The method of claim 38 further comprising:

performing a cell source/drain (S/D) implant to form the cell source and drain regions; and

after said cell S/D implant and said LDD implant and said DDD implant, performing a transistor S/D implant to form highly doped regions within all the DDD and LDD regions.

48. The method of claim 47 further comprising:

after said cell S/D implant and said LDD implant and said DDD implant but before said transistor S/D implant, forming main spacers adjacent the off-set spacers of at least the first and second transistors,

wherein the highly doped regions within all the DDD and LDD regions are of the same conductivity type as and have a doping concentration greater than the DDD and LDD regions.

49. The method of claim 48 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions, and the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers,

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers,

and the extent of an overlap between the polysilicon stack and the cell source and drain regions is inversely dependent on a thickness of the off-set spacers.

50. The method of claim 48 further comprising:

forming a cell DDD source region during said DDD implant so that said cell S/D implant forms a highly doped region within the cell DDD source region.

51. The method of claim 48 wherein N^- type impurities is used in said DDD implant and said LDD implant, and N^+ type impurities is used in said cell S/D implant and said transistor S/D implant.

52. The method of claim 48 wherein P^- type impurities is used in said DDD implant and said LDD implant, and P^+ type impurities is used in said cell S/D implant and said transistor S/D implant.

53. The method of claim 38 wherein said off-set spacers forming act is performed after said DDD implant but before said LDD implant.

54. The method of claim 53 further comprising:

after said LDD implant, forming main spacers adjacent the off-set spacers of at least the second transistor.

55. The method of claim 54 further comprising:

after said main spacers forming act, performing a source/drain (S/D) implant to form at least one of:

(a) cell source and cell drain regions, and

(b) highly doped regions within all the DDD and LDD regions.

wherein the highly doped regions within all the DDD and LDD regions are of the same conductivity type as and have a doping concentration greater than the DDD and LDD regions.

56. The method of claim 55 wherein,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacers only,

the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the off-set spacers, and

the extent of an overlap between the polysilicon stack and the cell source and drain regions is inversely dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacers only.

57. The method of claim 55 further comprising:

forming a cell DDD source region during said DDD implant so that said S/D implant forms a highly doped region within the cell DDD source region.

58. The method of claim 53 further comprising:

performing a cell source/drain (S/D) implant to form the cell source and drain regions; and

after said cell S/D implant, performing a transistor S/D implant to form highly doped regions within all DDD and LDD regions.

59. The method of claim 58 further comprising:

after said cell S/D implant but before said transistor S/D implant, forming main spacers adjacent the off-set spacers of at least the second transistor,

wherein the highly doped regions within all the DDD and LDD regions are of the same conductivity type as and have a doping concentration greater than the DDD and LDD regions.

60. The method of claim 59 wherein,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacers only,

the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the off-set spacers, and

the extent of an overlap between the polysilicon stack and the cell source and drain regions is inversely dependent on a thickness of the off-set spacers.

61. The method of claim 59 further comprising:

forming a cell DDD source region during said DDD implant so that said cell S/D implant forms a highly doped region within the cell DDD source region.

62. The method of claim 38 wherein said off-set spacer forming act is performed after both said DDD implant and said LDD implant.

63. The method of claim 62 further comprising:

performing a cell source/drain (S/D) implant to form the cell source and drain regions; and

after said cell S/D implant, performing a transistor S/D implant to form highly doped regions within all DDD and LDD regions.

64. The method of claim 63 further comprising:

after said cell S/D implant but before said transistor S/D implant, forming main spacers adjacent the off-set spacers of at least the second transistor,

wherein the highly doped regions within all the DDD and LDD regions are of the same conductivity type as and have a doping concentration greater than the DDD and LDD regions.

65. The method of claim 64 wherein,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacers only,

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacers only, and

the extent of an overlap between the polysilicon stack and the cell source and drain regions is inversely dependent on a thickness of the off-set spacers.

66. The method of claim 64 further comprising:

forming a cell DDD source region during said DDD implant so that said cell S/D implant forms a highly doped region within the cell DDD source region.

67. The method of claim 62 further comprising:

after said off-set spacers forming act, performing a source/drain (S/D) implant to form at least one of:

(a) cell source and cell drain regions, and

(b) highly doped regions within all the DDD and LDD regions.

wherein the highly doped regions within all the DDD and LDD regions are of the same conductivity type as and have a doping concentration greater than the DDD and LDD regions.

68. The method of claim 67 wherein,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the off-set spacers, and

the extent of an overlap between the polysilicon stack and the cell source and drain regions is inversely dependent on a thickness of the off-set spacers.

69. The method of claim 67 further comprising:

forming a cell DDD source region during said DDD implant so that said cell S/D implant forms a highly doped region within the cell DDD source region.

70. The method of claim 35 wherein the off-set spacers are from oxide or oxynitride.

71. The method of claim 35 wherein,

said off-set spacers forming act further comprises forming a first layer of insulating material over the polysilicon stack including its side-walls, the gate electrodes of the first and second transistors including their side-walls, and over exposed body regions; and

said at least one source and drain regions forming act further comprises implanting impurities through the insulating layer to form said source and drain regions for each of the memory cell and the first and second transistors.

72. The method of claim 35 wherein said off-set spacer forming act further comprises:

forming a first layer of insulating material over the polysilicon stack, the gate electrodes of the first and second transistors, and exposed semiconductor body region;

forming a second layer of insulating material different from the first layer of insulating material over the first layer of insulating material; and

etching at least the second layer of insulating material to form off-set spacers along the side-walls of the polysilicon stack and the gate electrodes of the first and second transistors.

73. The method of claim 72 wherein the first layer of insulating material is oxide and the second layer of insulating material is nitride, the etching act further comprising:

etching said first and second layers of insulating material so that only oxide-nitride off-set spacers remain along the side-walls of the polysilicon stack.

74. The method of claim 72 wherein the first layer of insulating material is oxide and the second layer of insulating material is nitride, the etching act further comprising:

etching only the nitride layer so that oxide-nitride off-set spacers are formed along the side-walls of the polysilicon stack and the gate electrodes of the first and second transistors while the nitride is removed from all other areas.

75. The method of claim 74 further comprising:

after said nitride layer etching act, implanting impurities through the oxide layer to form said source and drain regions for each of the memory cell and the first and second transistors.

76. The method of claim 35 wherein a thicker off-set spacer results in a smaller overlap between the polysilicon stack and the cell source and drain regions, and also results in a smaller overlap between each of the gate electrodes of the first and second transistors and their corresponding source and drain regions.

77. A structure comprising:

a first transistor comprising:

a first gate electrode over but insulated from a semiconductor body region;

off-set spacers along side-walls of the first gate electrode; and

a source region and a drain region in the body region so that the extent of an overlap between the first gate electrode and each of the source and drain regions is dependent on a thickness of the off-set spacers.

78. The structure of claim 77 further comprising:

a second transistor comprising:

a second gate electrode over but insulated from a semiconductor body region;

off-set spacers along side-walls of the second gate electrode;

source and drain regions; and

main spacers adjacent the off-set spacers of the first and second transistors;

wherein each of the source and drain regions of the first transistor comprises a highly doped region within a DDD region, and each of the source and drain regions of the second transistor comprises a highly doped region within a LDD region, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

79. The structure of claim 78 wherein the extent of an overlap between the first gate electrode and each of the DDD source and DDD drain regions, and the extent of an overlap between the second gate electrode and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers.

80. The structure of claim 79 wherein,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers, and

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is dependent on a thickness of the main spacers.

81. The structure of claim 80 wherein the DDD and LDD regions are from N^- type impurities, and the highly doped regions within the DDD and LDD regions are from N^+ type impurities.

82. The structure of claim 80 wherein the DDD and LDD regions are from P^- type impurities, and the highly doped regions within the DDD and LDD regions are from P^+ type impurities.

83. The structure of claim 78 wherein the extent of an overlap between first gate electrode and each of the DDD source and DDD drain regions is inversely dependent on a thickness of the off-set spacers, and the extent of an overlap between the second gate electrode and each of the LDD source and LDD drain regions is inversely dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacer only.

84. The structure of claim 83 wherein a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers.

85. The structure of claim 77 further comprising:

a second transistor comprising:

a second gate electrode over but insulated from a semiconductor body region;

off-set spacers along side-walls of the second gate electrode;

source and drain regions; and

main spacers adjacent the off-set spacers of the first and second transistors;

wherein each of the source and drain regions of the first transistor comprises a highly doped region within a LDD region, and each of the source and drain regions of the second transistor comprises a highly doped region within a DDD region, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

86. The structure of claim 85 wherein the extent of an overlap between the first gate electrode and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers.

87. The structure of claim 86 wherein,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on combined thickness of the off-set and main spacers or on a thickness of the off-set spacer only, and

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers.

88. The structure of claim 85 wherein the off-set spacers are from oxide, or oxynitride, or a composite layer of oxide-nitride wherein the nitride is the outer layer, or a composite layer of oxide-nitride-oxide wherein the nitride is the middle layer.

89. The structure of claim 85 wherein thicker off-set spacers result in smaller overlap between the first gate electrode and each of the source and drain regions.

90. A non-volatile memory cell comprising:

a first polysilicon layer over but insulated from a semiconductor body region;

a second polysilicon layer over but insulated from the first polysilicon layer;

an off-set spacer along at least one side-wall of the first and second polysilicon layers; and

source and drain regions in the body region, wherein the extent of an overlap between the first polysilicon layer and at least one of said source and drain regions is dependent on a thickness of the off-set spacer.

91. The memory cell of claim 90 wherein the first and second polysilicon layers form a polysilion stack, the memory cell further comprising off-set spacers along side-walls of the polysilicon stack so that the extent of an overlap between the polysilicon stack and each of the source and drain regions is inversely dependent on a thickness of the off-set spacers.

92. The memory cell of claim 90 where the non-volatile memory cell is a split gate cell.

93. The memory cell of claim 90 wherein the first and second polysilicon layers form a polysilion stack, the memory cell further comprising off-set spacers along side-walls of the polysilicon stack, said at least one of source and drain regions being a DDD source region, said DDD source region including a highly doped region, the highly doped region being of the same conductivity type as and having a doping concentration greater than the DDD source region.

94. The memory cell of claim 93 wherein the extent of an overlap between the polysilicon stack and each of the DDD source region, the highly doped region within the DDD source region, and the drain region is inversely dependent on a thickness of the off-set spacers.

95. The memory cell of claim 93 wherein the extent of an overlap between the polysilicon stack and each of the drain region and the region within the DDD source region is inversely dependent on a thickness of the off-set spacers, and a distance between an outer edge of the DDD source region and the highly doped region within the DDD source region is directly dependent on the thickness of the off-set spacers.

96. The memory cell of claim 95 wherein the DDD source region is from N^- type impurities, and the highly doped region within the DDD source region and the drain region are from N^+ type impurities.

97. The memory cell of claim 95 wherein the DDD source region is from P^- type impurities, and the highly doped region within the DDD source region and the drain region are from P^+ type impurities.

98. The memory cell of claim 90 wherein the off-set spacer is from oxide, or oxynitride, or a composite layer of oxide-nitride wherein the nitride is the outer layer, or a composite layer of oxide-nitride-oxide wherein the nitride is the middle layer.

99. The memory cell of claim 90 wherein a thicker off-set spacer results in a smaller overlap between the first polysilicon layer and the at least one of source and drain regions.